SILICON WAFER AND SILICON EPITAXIAL WAFER AND PRODUCTION METHODS THEREFOR

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Cited documents:

US5961713
JP62202528
JP63090141
JP5058788
JP3185831
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Abstract of **WO0225717**

A silicon wafer having a DZ layer in the vicinity of the surface thereof and an oxygen deposition layer in a bulk unit, wherein each of interstitial oxygen concentrations in the DZ layer, the oxygen deposition layer and in a transition layer between the DZ layer and the oxygen deposition layer is up to 8 ppma; a silicon epitaxial wafer having an epitaxial layer formed on the surface of this silicon wafer; and a production method of a silicon wafer, comprising the steps of growing a silicon single-crystal rod having an initial interstitial oxygen concentration of 10-25 ppma by a CZ method, processing the silicon single-crystal rod into a wafer, and subjecting the wafer to a first heat treating at 950-1050 DEG C for 2-5 hours, a second heat treating at 450-550 DEG C for 4-10 hours, a third heat treating at 750-850 DEG C for 2-8 hours, and a fourth heat treating at 950-1100 DEG C for 8-24 hours, whereby providing the production method of a silicon wafer capable of ensuring a high resistivity despite a device production heat treating.